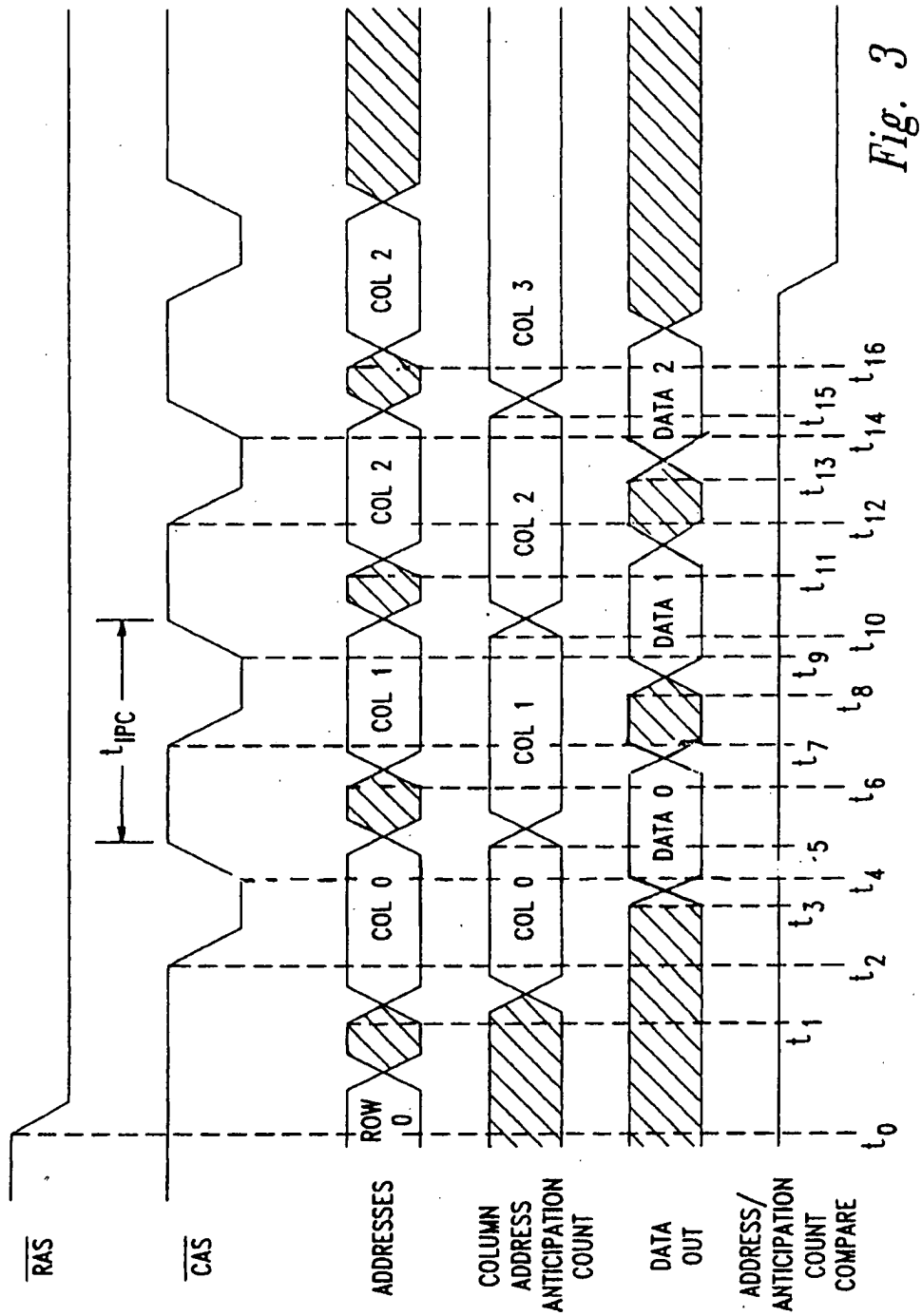
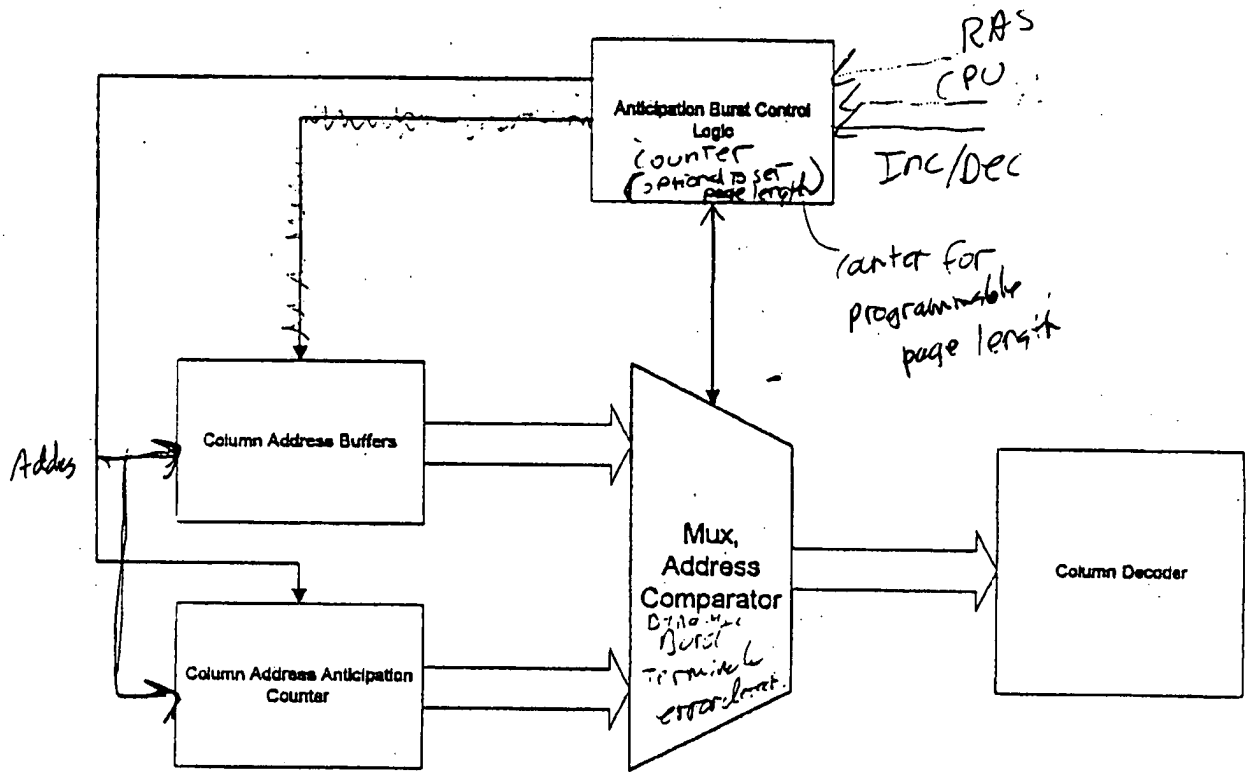


Fig. 3



Memory System Speed Enhancement
Block Diagram

Erik Erlandson, David Tremblay

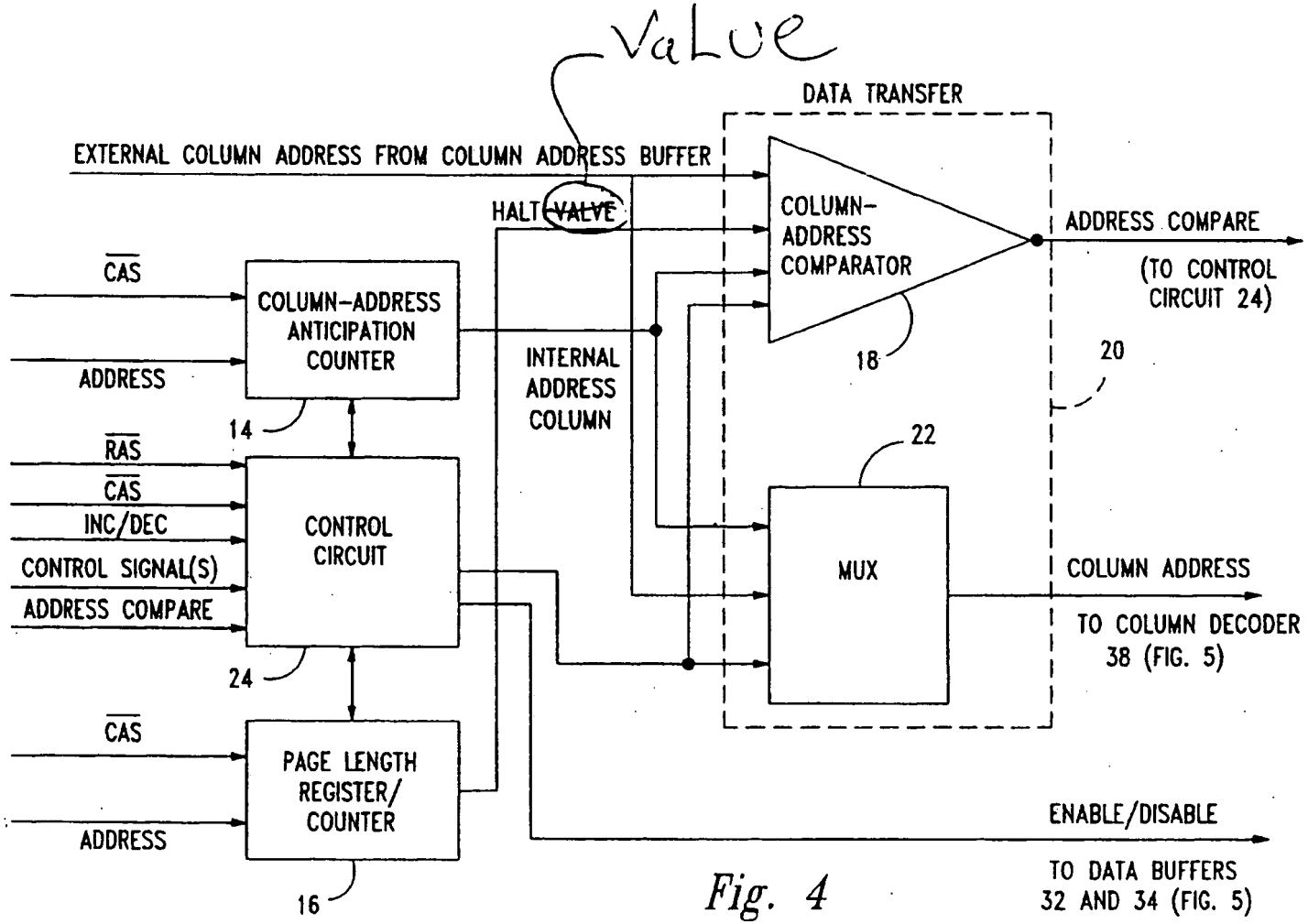


Fig. 4